REMARKS

Favorable reconsideration of this application in light of the following remarks is respectfully requested. Claims 1-11 are currently pending.

In the Office Action dated January 16, 2004, claims 1, 4, and 7 were rejected under 35 U.S.C. § 103(a) as being unpatentable over the combination of U.S. Patent 6,083,849 to Ping et al. ("Ping") in view of U.S. Patent 6,475,815 to Nambu et al. ("Nambu"); claims 5 and 9 were rejected under 35 U.S.C. § 103(a) as being unpatentable over the combination of Ping, Nambu, and U.S. Patent 6,348,367 to Ohtani et al. ("Ohtani"); claims 2 and 6 were rejected under the combination of Ping, Nambu, Ohtani, and U.S. Patent 6,240,610 to Ishihara et al. ("Ishihara"); claims 3 and 8 were objected to as being dependent upon a rejected base claim; and claims 10 and 11 were deemed allowed. Applicant appreciates the indication of the allowance of the subject matter of claims 3, 8, 10, and 11. The rejections of claims 1, 2, 4-7, and 9 are traversed for the following reasons.

Preliminarily, Applicant wishes to thank Examiner Estrada and Examiner Fourson for the courtesy of an interview granted to Applicant's representative, Jonathan Hack, on May 12, 2004. During the interview, Applicant's representative presented arguments detailing how the cited references do not disclose recited claims. Examiner Estrada indicated that she would reconsider the outstanding grounds for rejection upon formal submission of these remarks. Accordingly, Applicant now submits in this response the remarks previously presented to the Examiner during the interview.

The Rejection of Claims 1, 4, and 7

In the Office Action, independent claim 1 and claims 4 and 7, which depend from claim 1, were rejected under 35 U.S.C. §103 (a) as being unpatentable over Ping in combination with Nambu. Applicant respectfully traverses this rejection.

The Office Action asserts that the combination of Ping and Nambu shows the elements recited in independent claim 1. Applicant respectfully disagrees. Neither Ping nor Nambu, separately or in combination disclose, *inter alia*, forming a dielectric layer on the amorphous region, the amorphous region being formed by exposing an upper surface of a silicon substrate to halogen species, as recited in claim 1.

Ping re-crystallizes the amorphous layer before a material is deposited on the re-crystallized amorphous layer. In particular, Ping discloses a method for making a capacitor that includes forming an amorphous silicon layer 20 by chemical vapor deposition ("CVD") over a silicon oxide layer 14 having an opining 16. *See* col. 3, lines 20-27 and Fig. 2. Subsequently, the amorphous silicon layer 20 is converted to hemispherical grain ("HSG") polysilicon layer 30. *See* col. 3, lines 36-40, col. 1, lines 26-28 and col. 5, lines 1-8. A dielectric layer 32 is formed immediately over the HSG polysilicon layer 30. *See* col. 4, lines 56-58. Accordingly, Ping fails to disclose or suggest forming a dielectric layer on the amorphous region, as recited in claim 1.

Nambu is primarily directed at a method of calibrating the temperature of a processing chamber by determining the correlation between the re-crystallization of an amorphous silicon layer and the temperature of the re-crystallized silicon. *See* col. 15, lines 26-34 and col. 15, lines 55-59. Nambu forms an amorphous layer by ion

implanting ions into a region of a silicon substrate and determines the correlation between the rate of re-crystallization of the amorphized silicon substrate and temperature. In one instance Nambu discloses that a refractory metal (such as a titanium film, a cobalt film, or a nickel film) can be deposited on the amorphous region. *See* col. 22, lines 26-32. In this instance, a laser anneal is performed, whereby a reaction proceeds between the refractory metal film and the amorphous region to form a silicide layer. *See* col. 22, lines 32-36. However, Nambu does not disclose or suggest forming a dielectric layer on the amorphous region, as recited in claim 1.

Further, there is no motivation to combine Ping's method of forming a capacitor with Nambu's temperature calibration technique. In particular, Ping discloses forming a capacitor whose bottom plate completely lines the sidewalls and the bottom surface of the trench 16 formed in the silicon oxide layer 14. Ping uses a blanket CVD to deposit the amorphous silicon layer 20 on the sidewalls and on the bottom surface of the trench 16 before re-crystallizing the amorphous silicon layer to form the HSG polysilicon layer 30. *See* Figs. 2 and 3. The blanket CVD technique allows the HSG polysilicon layer, which forms the bottom capacitor plate, to have a large surface area. Further, the blanket CVD technique allows easy electrical connection to the HSG polysilicon layer.

In contrast, Nambu forms an amorphous silicon layer by ion implanting ions into the surface of a semiconductor substrate. However, using ion implantation to form the amorphous silicon layer in Ping would result in the bottom plate of the capacitor being formed only along the bottom surface of the trench 16 formed in the silicon oxide layer 14. In particular, ion implantation into the sidewalls of trench 16 (the sidewalls being silicon oxide) could not form an amorphous silicon layer. Rather, the ion implanted

sidewalls would form an amorphous silicon oxide layer, which is not an amorphous silicon layer. As such, one of ordinary skill in the art would not have been motivated to combine the method described in Nambu with the method described in Ping. Accordingly, Applicant respectfully submits Ping and Nambu, either singly or in combination, fail to disclose claim 1, as recited, and submits that claim 1 is in condition for allowance.

In addition, claims 4 and 7 depend from claim 1, and thus, are allowable for at least the same reasons that claim 1 is allowable, as well as for their additional recitations. Therefore, Applicant respectfully submits that claims 4 and 7 are also allowable over Ping and Nambu, either separately or in combination.

The Rejection of Claims 2 and 6

Claims 2 and 6 were rejected under 35 U.S.C. 103(a) as being unpatentable over Ping, Nambu, Ohtani, and Ishihara. Applicant respectfully disagrees. In particular, neither Ohtani nor Ishihara correct the deficiencies of Ping and Nambu with respect to independent claim 1, from which claims 2 and 6 depend. In particular, Ohtani discloses depositing an amorphous silicon film 203 on a silicon oxide film 202. *See* col. 9, lines 56-61. Subsequently, a solution containing nickel is deposited on the surface of the amorphous silicon film 203 "for accelerating the crystallization" of the amorphous silicon film. *See* col. 9, line 66 through col. 10, line 2. Thereafter, the amorphous silicon film is crystallized. *See* col. 10, lines 6-8. Any subsequent material will be formed over the crystallized silicon. *See*, for example, col. 10, lines 33-43.

Further, Ishihara is directed to maintaining a clean silicon substrate surface while the silicon substrate is transported for processing. *See* col. 1, lines 8-15. Ishihara also discloses methods of controlling native oxide growth on a silicon substrate. However, Ishihara fails to disclose or suggest forming a dielectric layer on the amorphous region, as recited in independent claim 1.

Accordingly, Applicant respectfully submits that Ohtani and Ishihara, either singly or in combination, fail to correct the deficiencies of Ping and Nambu in the rejection of independent claim 1, from which claims 2 and 6 depend. Therefore Applicant respectfully submits that claims 2 and 6 are in condition for allowance.

The Rejection of Claims 5 and 9

Claims 5 and 9 were rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Ping, Nambu, and Ohtani. Applicant respectfully disagrees. Neither Ping, Nambu, nor Ohtani disclose, *inter alia*, either forming a dielectric layer on the amorphous region, the amorphous region being formed by exposing an upper surface of a silicon substrate to halogen species, as recited in independent claim 1, the claim from which claim 9 depends, or forming a capping layer on an amorphous region, as recited in claim 5.

As shown above, Ping discloses forming a dielectric layer 32 immediately over the HSG polysilicon layer 30. *See* col. 4, lines 56-58. Nambu discloses forming a refractory metal (such as a titanium film, a cobalt film, or a nickel film) on the amorphous reigon. *See* col. 22, lines 26-32. Thereafter, a laser anneal is performed, whereby a reaction proceeds between the refractory metal film and the amorphous region to form a

silicide layer. *See* col. 22, lines 32-36. Further, Ohtani discloses depositing an amorphous silicon film 203 on a silicon oxide film 202. *See* col. 9, lines 56-61. Subsequently, a solution containing nickel is deposited on the surface of the amorphous silicon film 203 "for accelerating the crystallization" of the amorphous silicon film. *See* col. 9, line 66 through col. 10, line 2. Thereafter, the amorphous silicon film is crystallized. *See* col. 10, lines 6-8. Any subsequent material will be formed over the crystallized silicon. *See*, for example, col. 10, lines 33-43.

Accordingly, Applicant respectfully submits Ping, Nambu, and Ohtani, either singly or in combination fail to disclose claim 5, as recited, or claim 9, as recited, and submit that claims 5 and 9 are in condition for allowance.

In view of the foregoing remarks, Applicant respectfully requests the reconsideration of this application and the timely allowance of the pending claims.

Please grant any extensions of time required to enter this response and charge any additional required fees to the Texas Instruments Deposit Account 20-0668.

Respectfully submitted,

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